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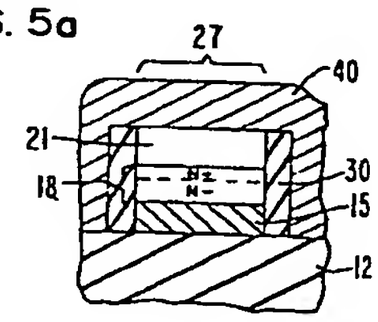
(54) Schottky diode - polycrystalline silicon resistor memory cell.

(57) A programmable integrated circuit structure useful for fabricating integrated circuit memory cells and a method of fabricating the cells are disclosed. The programmable structure includes a serially connected Schottky diode and a resistor formed by a region of intrinsic polycrystalline silicon. The resistance of the resistor is irreversably changeable by application of a suitably high threshold voltage. Application of such a voltage changes the characteristics of the resistor permanently, thereby providing a means for the storage of information.

FIG. 5a



EP 0 065 916 A2

SCHOTTKY DIODE - POLYCRYSTALLINE SILICON RESISTOR MEMORY CELL

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to integrated circuit structures and processes for fabricating them, and in particular to a compact series connected resistor and diode which may be used as a read only memory cell.

Description of the Prior Art

Conventional programmable read only memories (PROM) use either P-N junction diodes or Schottky diodes in series with a fuse. Unfortunately, as the number of such devices increases, the capacitance of the P-N junctions increase and slow the operating speed of the overall memory array. Furthermore, because the fusing elements require more wafer surface area than do the diodes, a PROM manufactured using such technology is much larger than a comparable ROM.

Another approach to the design of memory cells within a PROM is suggested in: "A Novel MOS PROM Using Highly Resistive Poly-Si Resistor," M. Tanimoto et al., IEEE Transactions on Electron Devices, Vol. ED-27, No. 3, March 1980, pages 517 - 520. That paper teaches use of a polycrystalline silicon resistor in conjunction with an MOS transistor as a memory element. There is no teaching, however, of the use of a polycrystalline silicon resistor in conjunction with a polycrystalline silicon Schottky diode or with an underlying low resistivity layer.

SUMMARY OF THE INVENTION

This invention relates to an integrated circuit structure in which a Schottky diode and a resistor are serially connected between a word line and a bit line in an array of memory cells. By fabricating the resistor from intrinsic polycrystalline silicon, the resistor will operate initially in a first highly resistive state. Application of sufficient potential across the resistor, however, will cause an irreversable change in the polycrystalline silicon to substantially lower the resistance of the resistor. The two states (high and low resistance) of the resistor may be used to store a binary bit of information.

In one embodiment an integrated circuit memory cell fabricated according to this invention includes an insulating substrate; a bottom layer of electrically conductive material disposed on the substrate; a plurality of intervening layers of semiconductor material disposed on the bottom layer, a selected layer of the plurality being substantially free of impurities; and an upper layer of electrically conductive material disposed on and in electrical contact with the uppermost of the plurality of intervening layers.

In one embodiment a method of fabricating an integrated circuit memory cell includes the steps of sequentially depositing on an insulating substrate a bottom layer of electrically conductive material; a plurality of intervening layers of semiconductor material, at least one of which is substantially free of impurities; and an upper layer of electrically conductive material in electrical contact with only the uppermost of the plurality of intervening layers. In the preferred embodiment the bottom layer is a metal silicide and the uppermost of the plurality of intervening layers is intrinsic polycrystalline silicon.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-section of an integrated circuit structure fabricated using well-known process steps.

Fig. 2 is a subsequent cross-sectional view after etching and oxidizing the structure shown in Fig. 1.

Fig. 3 is a subsequent cross-sectional view after deposition of a layer of metal across the surface of the structure.

Fig. 4 is a top view of the structure shown in Fig. 3.

Fig. 5a and Fig. 5b are cross-sectional views showing two embodiments of the memory cell.

Figs. 6a and 6b are schematic drawings of the circuits created by the structures depicted in Figs. 5a and 5b, respectively.

Fig. 7 is a graph illustrating the two states which each of the structures shown in Fig. 5a and 5b may have.

Fig. 8 is a graph showing the voltage required to cause the polycrystalline silicon resistor to change state as a function of thickness.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 is a cross-sectional view of an integrated circuit structure which may be fabricated using well-known technology. On an insulating substrate 12, typically silicon dioxide, a layer 15 of metal silicide is deposited. Typically the insulating substrate 12 will comprise a layer of silicon dioxide formed on an underlying region of silicon in which other electronic components, both active and passive, may be fabricated. In the preferred embodiment the metal silicide is tungsten silicide deposited using chemical vapor deposition to a thickness of 1,000 angstroms. On the upper surface of tungsten silicide 15 a layer of semiconductor material 18 is deposited. In the preferred embodiment layer 18 is chemical vapor deposited polycrystalline silicon 2,000 angstroms thick. After deposition, phosphorous or another N conductivity type impurity is implanted into layer 18 to lightly dope it to an impurity concentration of about 10^{17} atoms per cubic centimeter. The upper portion of layer 18, typically the top 1,000 angstroms, is more heavily doped by ion implantation with N type impurity, for example to a concentration of 10^{20} atoms per cubic centimeter. As will be evident, layer 15 provides an electrical connection to layer 18, while the more heavily doped portion of layer 18 provides

an electrical connection between the lower portion of layer 18 and an overlying layer formed on the upper surface of layer 18.

On the upper surface of layer 18 another layer of semiconductor material 21 is deposited. Layer 21 will typically be intrinsic polycrystalline silicon, and accordingly will have very high resistivity. Layer 21 is deposited by chemical vapor deposition to a thickness of about 3,000 angstroms. On the upper surface of layer 21 a relatively thin layer of silicon dioxide 23 is formed, typically by a thermal process. In the preferred embodiment layer 23 is 200 angstroms thick and is created by heating the underlying structure to a temperature of 1,000°C for 10 minutes in oxygen.

A layer 25 of silicon nitride approximately 1,000 angstroms thick is then formed using chemical vapor deposition. Nitride 25 prevents further oxidation of the upper surface of semiconductor material 21 during subsequent processing.

Using well-known integrated circuit fabrication technology, the structure shown in Fig. 1 is patterned into one or more strips 27a, 27b, etc. In the preferred embodiment this is accomplished by masking and etching silicon nitride layer 25 to remove it from everywhere except where the strips 27a and 27b are desired. Following this step the remaining regions 25b and 25d of nitride layer 25 themselves serve as a mask for the removal of all underlying materials down to the surface of the insulating substrate 12. In the preferred embodiment, the undesired portions of the layers underlying silicon nitride 25 are removed by sequentially plasma etching them, for example, with etch gases containing CF_4 and CCl_4, respectively. Because the plasma etching proceeds anisotropically, the strips will have substantially vertical side walls 28a, 28b, 28c, and 28d. Isotropic etching processes, for example etching with appropriate solutions, may also be employed to remove the undesired portions of layers 15, 18, 21, and 23, thereby leaving silicide regions 15b and 15d, polycrystalline silicon

18b, 18d, 21b and 21d, and silicon dioxide 23b and 23d, respectively.

Following the definition of strips 27a, etc., the structure is oxidized to create regions of silicon dioxide 30a, 30b, 30c, and 30d. These regions of silicon dioxide will later serve to prevent short circuiting between an overlying metal layer and the sides of layers 15, 18 and 21. The resulting conductive strips as shown in Fig. 2 are termed bit lines herein. As will be explained, a subsequently formed strip of metal as shown in Fig. 3 will create a word line. Upon application of a desired potential to the word line, the state of any cell on that word line may be determined by sensing the condition of that cell's bit line, or vice versa. Of course the terms "bit" and "word" are arbitrarily chosen and could be interchanged.

The silicon nitride 25 is then removed from the upper surface of the strips 27 and a layer of silicon dioxide 32 is thermally formed on the upper surface of silicon dioxide 23. Layer 32 is not shown in Fig. 3 because, as will be explained, it is subsequently removed. Layer 32 is shown in Fig. 4. Silicon dioxide 32 will be approximately 1,000 angstroms thick and formed by heating the structure to a temperature of 1,000°C for 60 minutes in steam.

As shown in Fig. 4, the silicon dioxide 32 is then removed from regions of the surface of the strips 27a and 27b to form windows 35a and 35b to expose underlying silicon layer 21. This may be accomplished using photolithographic techniques to define windows 35, followed by dip etching the oxide in a 10:1 dilute solution of H_2O and HF. Finally, as shown in Figs. 3 and 4, a layer of metal 40, typically aluminum 7,000 angstroms thick, is deposited across the surface of the structure and defined into word lines extending generally perpendicular to the bit lines.

Fig. 4 is a top view of the structure shown in Fig. 3. The word line 40 crosses bit lines 27a and 27b, and as shown, is in electrical contact with silicon 21b and silicon 21d through windows 35a and 35b in silicon dioxide 32b and 32d.

Figs. 5a and 5b illustrate two embodiments of the invention, with Fig. 5a illustrating the embodiment described in conjunction with Figs. 1 to 4. In the embodiment shown in Fig. 5b, the arrangement of the layers in the strip 50 is different from that depicted in strip 27 in Fig. 5a. In strip 50 an underlying layer of tungsten silicide 51 is formed on the surface of silicon dioxide 12. A heavily doped layer of polycrystalline silicon 53 about 1,000 angstroms thick is formed on metal silicide 51, followed by a layer of intrinsic polycrystalline silicon 55 approximately 3,000 angstroms thick. A layer of lightly doped polycrystalline silicon 57 about 2,000 angstroms thick is deposited on layer 55. In the preferred embodiment, to provide a better connection between layers 57 and 40 the upper layer 57 of polycrystalline silicon will be laser annealed. An alternate technique for fabricating the embodiment shown in Fig. 5b is to deposit layers 53, 55 and 57 as a single thick layer, and then use ion implantation to create the desired impurity doping. The impurity concentrations for layers 53, 55 and 57 in Fig. 5b correspond to those for the upper portion of layer 18, layer 21 and the lower portion of layer 18, respectively, in Fig. 5a.

For the structure shown in Fig. 5a, the Schottky diode is created by the interface between layer 18 and layer 15, while layer 21 functions as a resistor. For the structure shown in Fig. 5b the Schottky diode is created by the interface between metal 40 and lightly doped polycrystalline silicon 57, while layer 55 functions as a resistor.

Figs. 6a and 6b are schematics of the memory cells shown in Figs. 5a and 5b, respectively. In each of Figs. 6a and 6b the programmable memory cell is connected between word line 40 and bit line 15 (Fig. 6a) or 51 (Fig. 6b). As is apparent from a comparison of Figs. 5 and 6, the primary difference between the different embodiments is the arrangement of the individual elements within the cell. In particular, the Schottky diode is connected to the word line and the resistor 55 is connected to the bit line in Figs. 5b and 6b. In Figs. 5a and 6a this arrangement is reversed.

Fig. 7 illustrates the current-voltage relationship of the polycrystalline silicon resistor 21 (in Fig. 5a) or 55 (in Fig. 5b). As shown, the resistor will operate in one of two states, termed herein a high resistance state and a low resistance state. In the high resistance state the resistor's charcteristics are shown in the designated curve in Fig. 7. For an applied voltage on the order of one volt, the current flow will be on the order of 10^{-9} amperes. At a particular threshold voltage (described in conjunction with Fig. 8), for example, that designated by the triangle, the current-voltage characteristics of the resistor will change dramatically and irreversibly to a low resistance state. This is designated in Fig. 7 by the curved line 60 connecting the high resistance state curve with the low resistance state curve. Once the threshold voltage is surpassed, the resistor will thereafter operate, regardless of the applied voltage, in the low resistance state. As shown by Fig. 7, the resistance of the resistor is several orders of magnitude greater in the high resistance state than in the low resistance state. As explained previously, the change of state of the resistor may be used to indicate a binary bit.

Although the precise mechanism by which the condition of the resistor irreversibly changes upon application of the suitably high threshold voltage is still unknown, it is understood that the transitional voltage depends upon the temperature at which the polycrystalline silicon resistor is formed and the thickness of the polycrystalline silicon. A typical relationship between transitional voltage and polycrystalline silicon thickness, for polycrystalline silicon formed at less than 700°C, is shown in Fig. 8. As indicated, for a thickness of 0.6 microns, the resistor will irrevocably change state upon application of approximately a 15 volt signal.

The change of state of the resistor may be most readily utilized in an array of memory cells by programming the desired cells with a suitably high potential to cause the resistors in those cells to change state. The memory array is then operated with potentials substantially lower than

this threshold voltage to sense the high or low resistance state of the individual resistors within the array.

Although several embodiments of the invention have been discussed herein, these embodiments are intended to be illustrative of the invention rather than limiting the invention, which is defined by the scope of the appended claims.

WHAT IS CLAIMED IS:

1. A method of fabricating an integrated circuit memory cell characterized by:

depositing a bottom layer of electrically conductive material on an insulating substrate;

sequentially fabricating a plurality of layers of semiconductor material on the bottom layer, a selected layer of the plurality of layers being substantially free of impurities; and

forming an upper layer of electrically conductive material in electrical contact with only the uppermost layer of the plurality of layers.

2. A method as in Claim 1 characterized in that the step of sequentially fabricating a plurality of layers comprises:

depositing a first layer on the bottom layer;

introducing a selected impurity into the first layer; and

depositing the selected layer on the first layer.

3. A method as in claim 1 or 2 characterized in that the uppermost layer is the selected layer.

4. A method as in Claim 2 or 3 characterized in that the selected layer and the first layer comprise polycrystalline silicon.

5. A method as in Claim 2, 3 or 4 characterized in that the selected impurity is not uniformly distributed throughout the first layer.

6. A method as in Claim 1 or 2 characterized in

that the bottom layer comprises metal silicide and the upper layer comprises metal.

7. A method as in Claim 6 characterized in that the metal silicide comprises tungsten silicide.

8. A method as in Claim 1 characterized in that the step of sequentially fabricating comprises:

depositing a first layer on the bottom layer;

introducing a selected impurity into the first layer;

depositing the selected layer on the first layer;

depositing a second layer on the selected layer; and

introducing the selected impurity into the second layer.

9. A method as in Claim 8 charcterized in that the second layer is the uppermost layer.

10. A method as in claim 8 or 9 characterized in that each of the first layer, the selected layer and the second layer comprise polycrystalline silicon.

11. A method of Claim 1 characterized in that in said plurality of layers of semiconductor material, said selected layer is intrinsic which is substantially free of impurities and in that one of said layers is doped which is selectively doped with an impurity; and further characterized by the steps of:

removing selected portions of the sequentially deposited layers to create at least one first strip of the sequentially deposited layers extending across the insulating substrate;

fabricating insulating material on the at least one strip to cover all of the strips except a desired

surface of the uppermost of the plurality of layers; and

forming a strip of second electrically conductive material which crosses the at least one strip and does not electrically contact any of the strip except the uppermost layer of the plurality of layers.

12. A method as in Claim 11 characterized in that the intrinsic layer is deposited on the doped layer.

13. A method as in Claim 11 or 12 characterized in that the doped layer includes a lower and an upper portion, the upper portion containing more of the impurity than the lower portion.

14. A method as in any one of Claims 11-13 characterized in that the strip of second electrically conductive material is substantially perpendicular to the at least one first strip.

15. A method as in any one of Claims 11-13 characterized in that the bottom electrically conductive layer comprises metal silicide and the second electrically conductive layer comprises metal.

16. A method as in Claim 15 characterized in that the metal silicide comprises tungsten silicide and the metal comprises aluminum.

17. A method as in Claim 11 characterized in that the doped layer is deposited on the intrinsic layer.

18. A method as in Claim 17 characterized in that a third layer separates the intrinsic layer from the first electrically conductive layer.

19. A method as in Claim 18 characterized in

that the third layer comprises polycrystalline silicon doped with the same impurity as the doped layer.

20. A method as in Claim 11 characterized by the step of depositing a layer of silicon nitride on the uppermost of the plurality of layers and subsequently removing the silicon nitride from regions of the uppermost of the plurality of layers wherever the strip of second electrically conductive material crosses the at least one strip.

21. A method of Claim 1 characterized in that the step of fabricating a plurality of layers includes:

depositing on the bottom layer a layer of semiconductor material having a lower and an upper surface;

introducing a selected impurity into the layer of semiconductor material to create a lower region of impurity near the lower surface and an upper region of impurity near the upper surface; and in that

the upper layer of electrically conductive material is in electrical contact with only the upper surface.

22. A method as in Claim 21 characterized in that the step of introducing an impurity comprises implanting ions of the impurity.

23. A method as in any one of Claims 1-20 characterized by the step of forming a contact area of the uppermost layer of the plurality of layers substantially self aligned vertically with its side edges for contacting the upper layer.

24. An integrated circuit memory cell structure characterized by:

an insulating substrate;

a bottom layer of electrically conductive material

disposed on the substrate;

a plurality of intervening layers of semiconductor material disposed one atop the other on the bottom layer, a selected layer of the plurality being substantially free of impurities; and

an upper layer of electrically conductive material disposed on and in electrical contact with only the uppermost layer of the plurality of intervening layers.

25. A structure as in Claim 24 characterized in that the uppermost layer is the selected layer.

26. A structure as in Claim 24 or 25 characterized in that the selected layer is separated from the bottom layer by a second layer of the plurality of intervening layers.

27. A structure as in Claim 26 characterized in that a selected impurity is distributed nonuniformly throughout the second layer.

28. A structure as in Claim 27 characterized in that more of the selected impurity is present in that portion of the second layer contiguous to the selected layer than in other portions of the second layer.

29. A structure as in any one of Claims 24-28 characterized in that the selected layer comprises intrinsic polycrystalline silicon.

30. A structure as in any one of Claims 26-29 characterized in that the second layer comprises polycrystalline silicon doped with an N conductivity type impurity.

31. A structure as in any one of claims 24-30 characterized in that the bottom layer comprises metal silicide.

32. A structure as in Claim 31 characterized in that the metal silicide comprises tungsten silicide.

33. A structure as in any one of Claims 24-32 characterized in that the upper layer comprises metal.

34. A structure as in any one of claims 24-33 characterized in that the insulating substrate comprises silicon dioxide.

35. A structure as in Claim 24 characterized in that a region of silicon dioxide separates the upper layer from all of the plurality of intervening layers except the uppermost layer.

36. A structure as in claim 24 characterized in that the plurality of intervening layers comprise the selected layer, a first layer, and a second layer.

37. A structure as in Claim 36 characterized in that the selected layer separates the first layer from the second layer.

38. A structure as in Claim 37 characterized in that the first layer is disposed on the bottom layer.

39. A structure as in Claim 38 characterized in that the first layer contains more of a selected impurity than the second layer, and the first layer provides an ohmic connection between the bottom layer and the selected layer.

40. A structure as in Claim 39 characterized in that the selected layer comprises intrinsic polycrystalline silicon and each of the first layer and the second layer comprise polycrystalline silicon doped with an N conductivity type impurity.

41. A structure as in any one of Claims 24-40 characterized in that the bottom layer and the upper layer comprise mutually perpendicular electrically conductive lines.

42. A structure as in any one of Claims 24-41 characterized in that the upper layer contacts the uppermost layer through a contact area of the uppermost layer self aligned vertically with its side edges.

FIG. 1

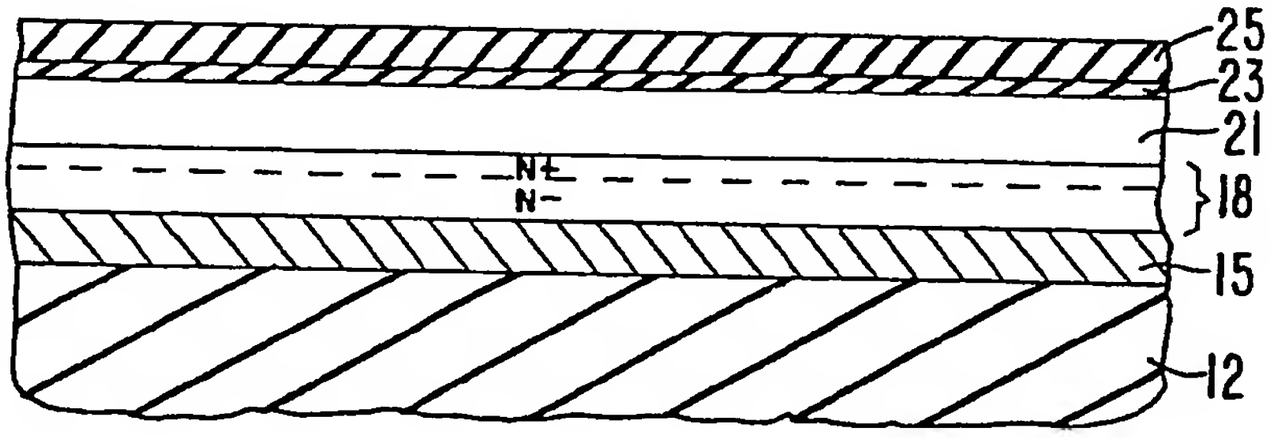


FIG. 2

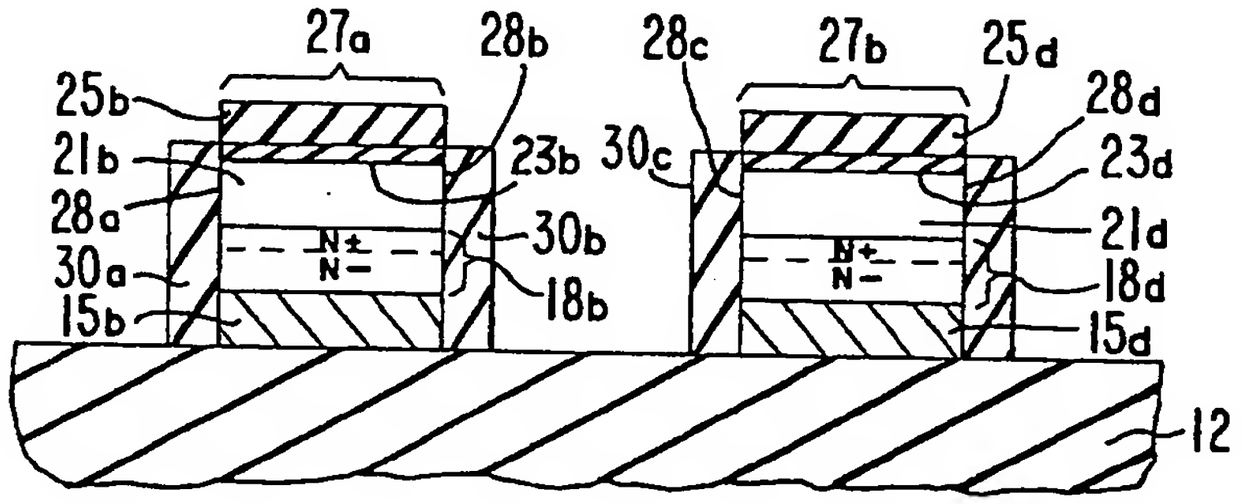


FIG. 3

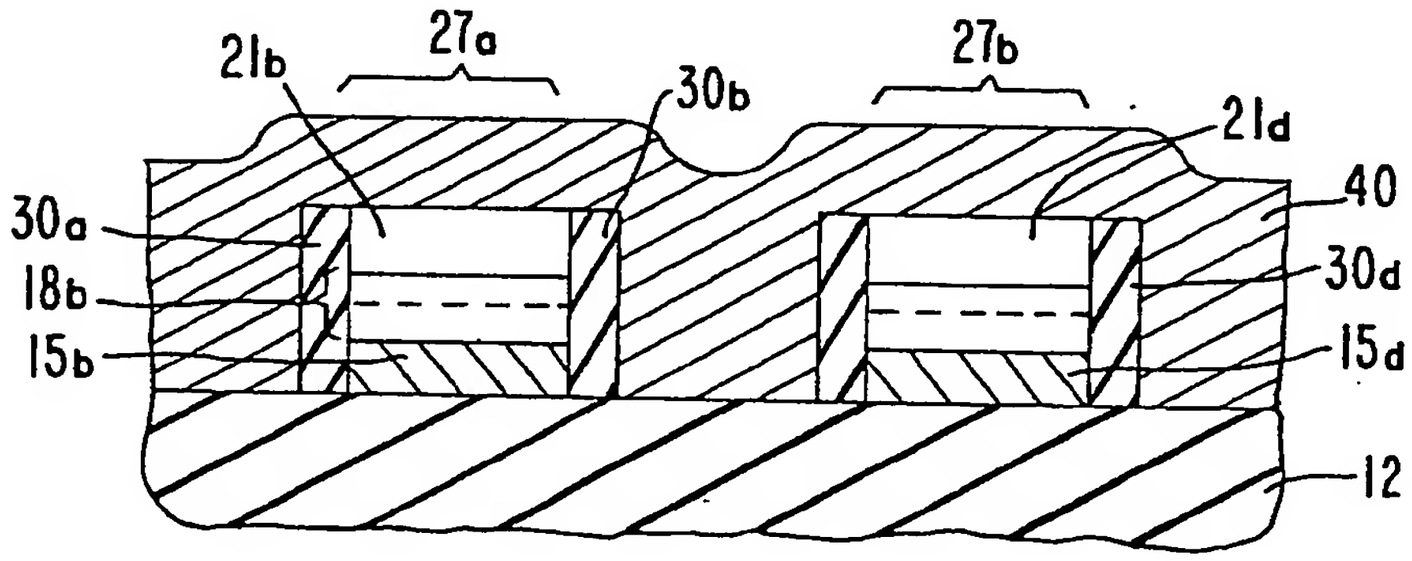


FIG. 4

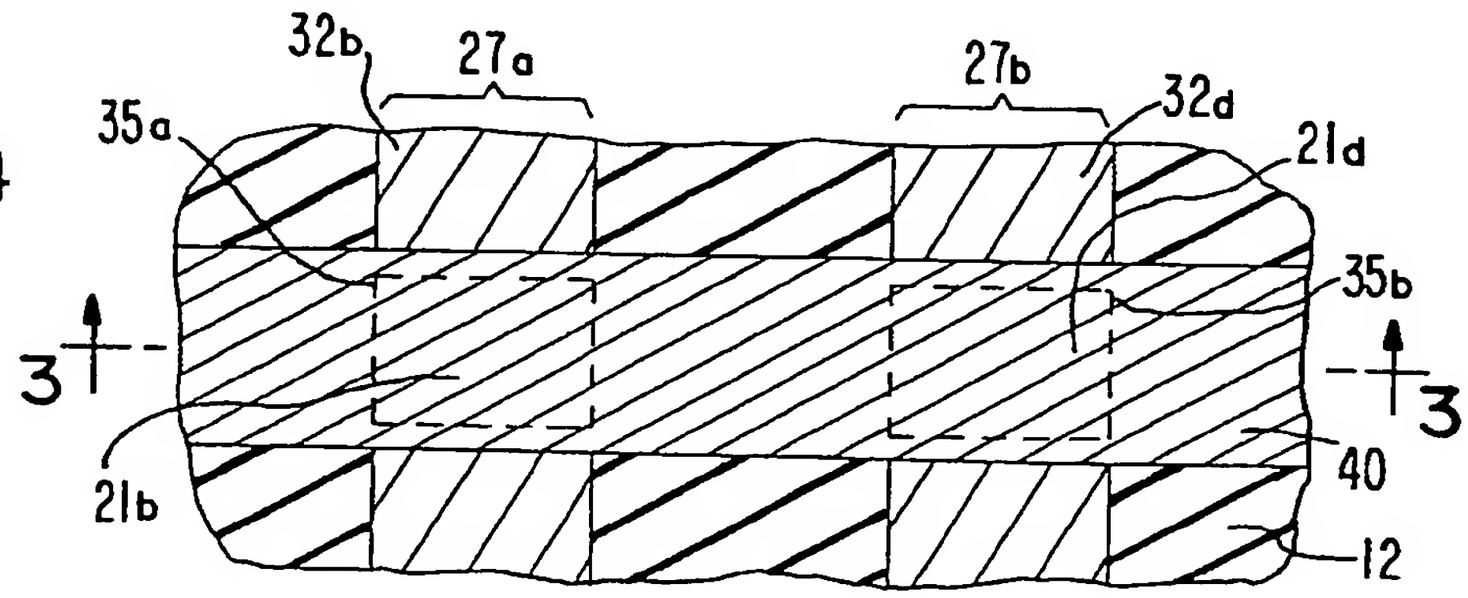


FIG. 5a

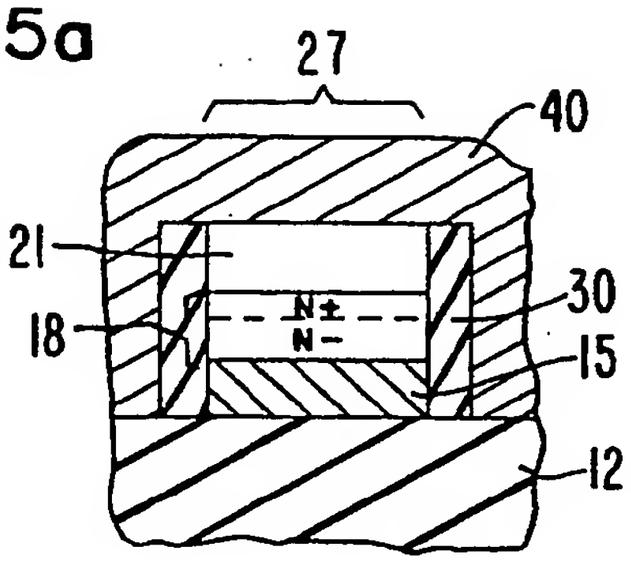


FIG. 5b

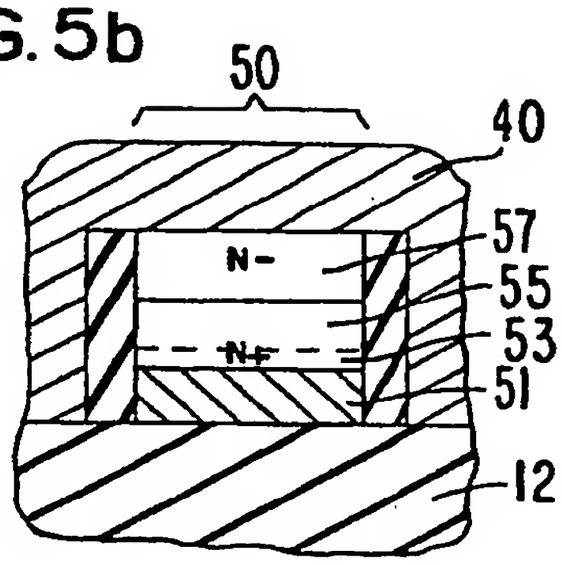


FIG. 6a

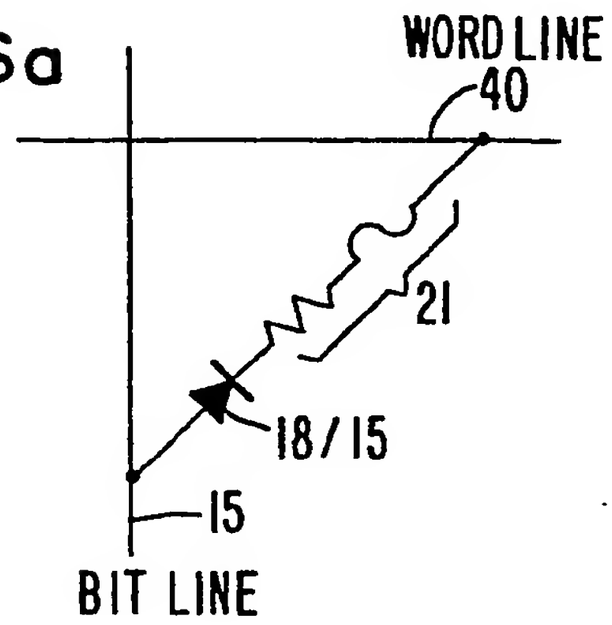


FIG. 6b

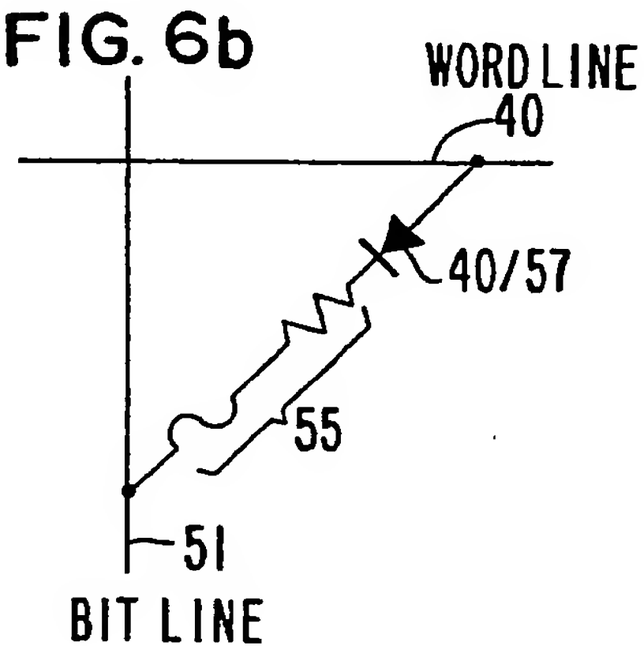


FIG. 7

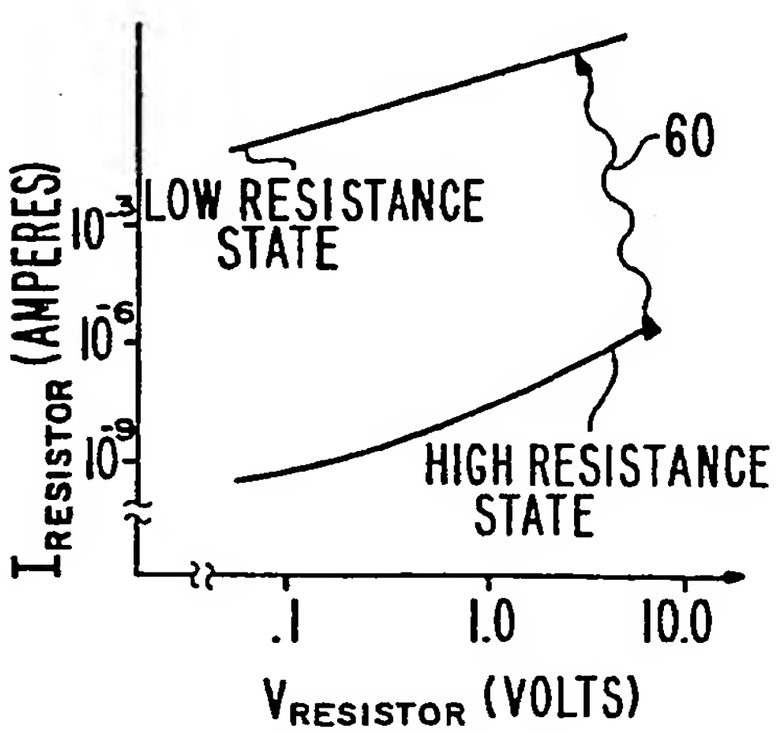
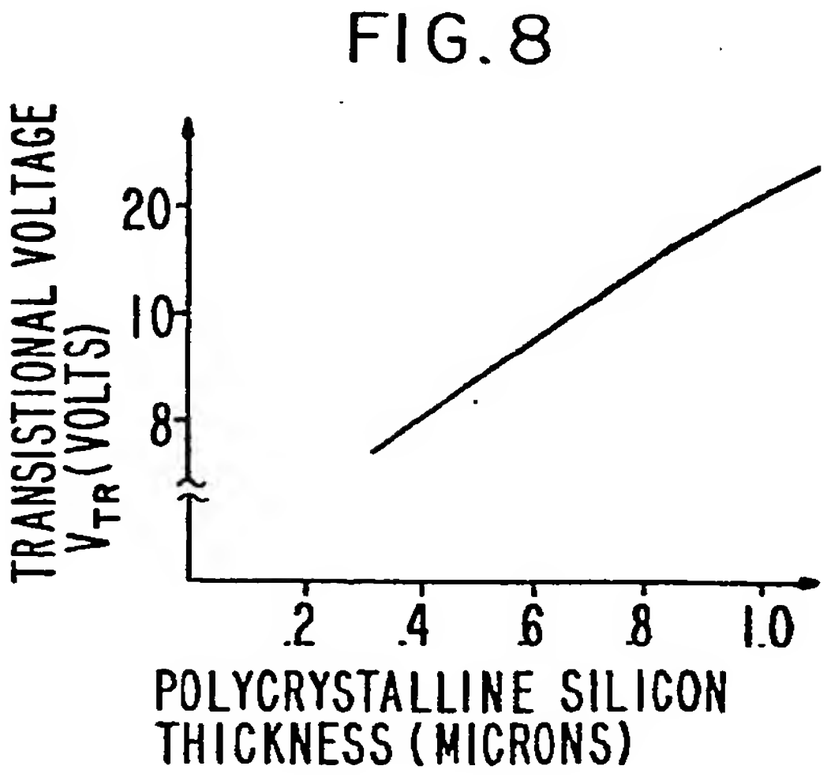


FIG. 8



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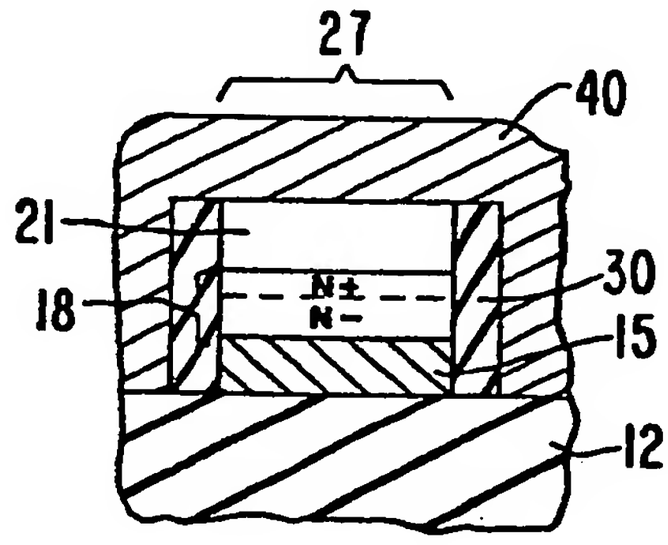
(54) **Schottky diode - polycrystalline silicon resistor memory cell.**

(57) A programmable integrated circuit structure useful for fabricating integrated circuit memory cells and a method of fabricating the cells are disclosed. The programmable structure includes a serially connected Schottky diode and a resistor formed by a region of intrinsic polycrystalline silicon. The resistance of the resistor is irreversably changeable by application of a suitably high threshold voltage. Application of such a voltage changes the characteristics of the resistor permanently, thereby providing a means for the storage of information.



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European Patent Office

EUROPEAN SEARCH REPORT

0065916
Application number

EP 82 40 0892

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. ³)
Y	US-A-4 203 123 (BURROUGHS CORP.) * claims 1,3; column 4, lines 25-63; column 5, line 42 - column 6, line 13; figures 3A,3B,7 *	1,3	G 11 C 17/00 H 01 L 27/12
Y	US-A-4 146 902 (NIPPON TELEGRAPH AND TELEPHONE PUBLIC CORP.) * claims 1-4, column 5, line 5 - column 6, line 18; figures 7,13 *	1-2,8-10	
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol.21, no.9, February 1979, New York (US) V.L. RIDEOUT: "Self-registering metal-to-polysilicon contacting technique", pages 3818-3821 * page 3820, paragraph 1 - page 3821, paragraph 1; figures 3A-3C *	11,20	
E,X	EP-A-0 058 748 (BURROUGHS CORP.) * claims 1-2, 4-7,10; page 24, line 29 - page 25, line 17; page 28, line 16 - page 30, line 30; figures 1-3,16 *	24-31, 33-42	

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TECHNICAL FIELDS SEARCHED (Int. Cl. ³)
H 01 L G 11 C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	13-01-1983	FRANSEN L.J.L.

EPO Form 1503. 03.82

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

European Patent Office

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DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. ³)
A	PATENTS ABSTRACTS OF JAPAN, vol.3, no.121, October 11, 1979, Page 56 E 143 & JP - A - 54 98 536 (NIPPON DENSHIN DENWA KOSHA) (03-08-1979) * abstract and figure *	24-25	
A	US-A-4 110 488 (RCA CORP.) * claims 1,2; column 4, line 29 - column 5, line 23; figure 1 *	1,5,6, 15	
A	US-A-3 515 583 (MATSUSHITA ELECTRONICS CORP.) * claim 1; column 2, lines 3-26 *	15,16	
			TECHNICAL FIELDS SEARCHED (Int. Cl. ³)

The present search report has been drawn up for all claims

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THE HAGUE	13-01-1983	FRANSEN L.J.L.

CATEGORY OF CITED DOCUMENTS

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